REMARKS

This paper is responsive to the Office Action mailed on October 23, 2003. Reconsideration of this application is respectfully requested. Claims 1-8 are currently pending in this application. Claims 2, 4-6, and 8 are original. Claims 1-8 and remain under consideration, and of these claims, claims 1, 3, 5, and 7 are independent. Claims 5-6 are allowed. There are no new claims. No new matter is added.

Claims 1, 3, and 7 have been amended to overcome the Examiner's objection. Specifically, the following informalities were objected to and amended. A period replaced a comma of claim 1. Claim 3 was amended to clarify the antecedent basis for "the mastership resolution unit." In claim 7, "a second signals" was changed to "a second signal." Accordingly, claims 1-2 should be a condition for allowance.

The Office Action rejects claims 3 and 7 under 35 U.S.C. §102(e) as being anticipated by U.S. Patent No. 6,614,752 (Parrish et al.). The Office Action rejects claims 4 and 8 under 35 U.S.C. §103(a) as being unpatentable over Parrish et al. in view of U.S. Patent No. 5,422,915 (Byers et al.).

Both Parrish and Byers concern what appears to be fault tolerant and/or redundant clocking mechanisms. They do not concern mastership determination.

For example, Parrish discloses the transition a standards-based card into a high availability backplane environment. The Parrish system had redundant clock busses with an "A" bus being initially used. When a failure is detected, the system transitions to the "B" bus. Col. 9, line 57 through Col. 10, line 15. The reference is silent as to how mastership is determined and simply says that service providers are first instructed to synchronize to one clock and then to the other. Parrish does not teach or suggest how mastership is determined.

Byers discloses a fault tolerant clock distribution system for providing synchronized clock signals to multiple circuit loads. Byers discloses redundant clock sources. Byers is silent with respect to how their redundant trace signals are analyzed by any form of mastership determination logic unit.

The rejected claims recite a specific system for indicating and determining a master unit from a plurality of logic units. Rejected claim 3, for example, recites a mastership determination

logic unit that is further configured to indicate whether the first or second logic unit is the master unit based on the first and second obey signals. As stated above, Parrish does not teach or suggest how mastership is controlled and thus does not teach or suggest a specific approach to such, such as that recited in claim 3. For example, Parrish does not teach how the system would determine which clock is master. If both clock busses are working, Parrish does not disclose how the system determines which is master.

Claim 7 recites a method for indicating and determining a master unit from a plurality of logic units including determining that the second logic unit is the master unit when the first and second signals are time varying and in which the signal is varying in-phase or out-of-phase. Parrish just discloses synchronization and doesn't make any determination based on whether a signal is in-phase or out-of-phase. The Examiner argues that a lost signal and an out-of-phase signal are synonymous. Applicants respectfully disagree. A lost signal has no phase and is not considered by one skilled in the art to be in-phase or out-of-phase even when those terms are construed broadly. An out-of-phase signal is well known in the art. The term only has meaning with respect to another signal. An signal is described as out-of-phase when the signal has a substantially similar waveform to another signal but is shifted in time (or phase).

Even if Parrish is interpreted as disclosing time or phase-varying clocks, Parrish does not teach which clock is dominant when comparing two clock that are out-of-phase. At best, a clock fault would result because Parrish's clocks are always supposed to be in-phase and synchronized. Therefore, Parrish does not teach or suggest "the first and second signals are time varying out-of-phase" as set forth in claim 7. As such, claim 7 distinguishes over the cited art.

Regarding claims 4 and 8 rejected under §103(a), neither Parrish nor Byers disclose redundant "obey signals" or analysis of such to determine mastership control. Since claims 4 and 8 depend, directly or indirectly, from independent claims 3 and 7, claims 4 and 8 should be allowed for at least the same reasons as provided for claims 3 and 7.

For at least the reasons stated in these Remarks, Applicants believe all pending claims to define patentable subject matter. An early and favorable examination result is earnestly solicited. Questions or issues arising in this matter should be directed to Applicants' representatives, listed below.

The Commissioner is authorized to charge Deposit Account No. 08-0219 the fee of $55.00 to cover the cost of the requested one month extension of time. No other fees are believed to be due in connection with this paper. However, please charge any fees, or credit any overpayment, that may be due in connection with this paper to Deposit Account No. 08-0219.

Respectfully submitted,

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